

**ABSTRACT OF THE DISCLOSURE**

This invention is directed to the reduction of voltage dependence and thus allows easy design of integrated semiconductor circuits. The device is equipped with a P – type resistance layer, in which a first voltage is applied to one end and a second voltage is applied to the other end and which is formed on the surface of an N-well region on the semiconductor substrate, a thin oxide film on the resistance layer , and a resistance bias electrode which includes the silicon layer formed on the thin oxide film. By adjusting the voltage applied to the resistance bias electrode, the voltage dependence of the resistance of the resistance layer is reduced.

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